Office Action Summary	Application No.	Applicant(s)	
	10/620,862	ANVIN ET AL.	
	Examiner	Art Unit	
	BENJAMIN P. GEIB	2181	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/20/2008 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4-10, 13-19, and 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dehnert et al., "The Transmeta Code Morphing Software: Using Speculation, Recovery, and Adaptive Retranslation to Address Real-Life Challenges" (Hereinafter Dehnert), in view of Gupta et al., U.S. Patent No. 5,881,280 (Hereinafter Gupta).

4. Referring to claim 1, Dehnert has taught in a computer system comprising a microprocessor, a method comprising:

operating in a first mode of speculative operation, said first mode permitting speculation of a first set of speculative operations *[1st and 2nd paragraphs of section 3]*;

experiencing an event during said operating *[exception; section 3.1]*;

in response to said event, restoring a state of said microprocessor to a state committed to memory prior to said event;

subsequent to said restoring, suspending a non-null first subset of said first set of speculative operations, wherein speculative operations in said first subset are not permitted during said suspending

[since execution from speculation boundary is done in-order, speculative operations are not permitted; section 3.1]; and

exiting said first mode and entering a second mode of speculative operation in response to said event *[exiting full speculation mode and executing from speculation boundary is in-order; section 3.1]* wherein said first subset input/output (I/O) writes *[4th paragraph of section 3.4]*, main memory reads *[2nd paragraph of section 3]*, and main memory writes *[2nd paragraph of section 3]*, wherein said first mode permits speculation for handling non-architectural faults, and wherein said second mode permits speculation for handling architectural faults.

Dehnert has not taught that the method provides partial speculative operation in lieu of suspending speculation wherein the second mode permits speculation of a non-null second subset of said first set, and wherein said second subset comprises operations that involve memory that is private to said microprocessor.

Gupta has taught a method that provides partial speculative operation in lieu of suspending speculation wherein executing according to a partial speculation mode that permits speculation on a first subset of operations and does not permit speculation on a second subset of operations and wherein the subset of operations that speculation is permitted upon comprises operations that involve memory that is private to a microprocessor *[Gupta; Speculation is permitted on all operations except those that are visible outside of the processor; column 6, line 45 – column 7, line 4]*.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify the method of Dehnert so that the method provides partial speculative operation in lieu of suspending speculation wherein the second mode permits speculation of a non-null second subset of said first set, wherein said second subset comprises operations that involve memory that is private to the microprocessor.

The motivation for doing so would have been that performance is increased by executing speculatively *[Gupta; column 1, lines 58-59]* while errors generated by operations that affect the state of external hardware are prevented *[Gupta; column 6, line 65 – column 7, line 4]*.

5. Referring to claims 4, 13, and 22, taking claim 4 as exemplary, Dehnert and Gupta have taught the method of Claim 1 wherein said second subset comprises speculative operations that are invisible external to said microprocessor *[Gupta; column 6, line 45 – column 7, line 4]*.

6. Referring to claims 5, 14, and 23, taking claim 5 as exemplary, Dehnert and Gupta have taught the method of Claim 1 wherein said event is selected from the group consisting of a fault, and a direct memory access request *[Dehnert; section 3.2]*.

7. Referring to claims 6 and 15, taking claim 6 as exemplary, Dehnert has taught the method of Claim 1 further comprising suspending speculative operation in response to a second event *[Dehnert; section 3.1]*.

8. Referring to claims 7, 16, and 24, taking claim 7 as exemplary, Dehnert and Gupta have taught the method of Claim 1 further comprising returning to said first mode after said event is handled *[Dehnert; section 3.1]*.

9. Referring to claims 8, 17, and 25, taking claim 8 as exemplary, Dehnert and Gupta have taught the method of Claim 1 further comprising: counting the number of instructions executed in said first mode prior to said event *[The number of instructions is counted using the program counter, which is inherently needed to correctly execute the program]*; and returning to said first mode upon executing the same number of instructions after entering said second mode *[Dehnert; The instructions corresponding to the faulting translation are executed (section 3.1). Therefore, at least the same number of instructions are executed]*.

10. Referring to claims 9, 18, and 26, taking claim 9 as exemplary, Dehnert and Gupta have taught the method of Claim 1 wherein said microprocessor *[Transmeta Crusoe microprocessor]* comprises a combination of translation software *[Code Morphing Software (CMS); See Fig. 1]* and host hardware *[VLIW processor; See 2nd paragraph of section 2]*, said translation software running directly on said host hardware, said translation software for interpreting and translating a sequence of non-native instructions *[x86 instructions]* into a sequence of native instructions *[VLIW instruction "molecule"] [See section 2]*.

11. Referring to claim 10, Dehnert has taught a method providing partial speculative operation, said method comprising:

executing forward from a speculation boundary *[start of a translation]* representing a memory state *[shadow register state]* of a microprocessor, said executing according to a full speculation mode that permits a set of speculative operations *[section 3.1]*;

experiencing an event *[exception]* during said executing *[section 3.1]*;

rolling back to said speculation boundary *[start of translation]* and restoring said memory state *[shadow register state]* in response to said event *[section 3.1]*;

subsequent to said rolling back, suspending a non-null first subset of said speculative operations, wherein speculative operations in said first subset are not permitted during said suspending *[since execution from speculation boundary is done in-order, speculative operations are not permitted; section 3.1]*;

subsequent to said suspending, executing forward from said speculation boundary non-speculatively *[execution from speculation boundary is done in-order and therefore non-speculatively; section 3.1]*.

wherein said first subset comprises input/output (I/O) writes *[4th paragraph of section 3.4]*, main memory reads *[2nd paragraph of section 3]*, and main memory writes *[2nd paragraph of section 3]*, wherein said full speculation mode permits handling non-architectural faults.

Dehnert has not taught that the first subset does not include all of said speculative operations. Dehnert has further not taught that the executing forward from said speculation boundary is according to a partial speculation mode that permits a non-null second subset of said set of speculative operations, wherein said partial speculation mode is used in lieu of suspending said set of speculative operations in entirety, and wherein said second subset comprises operations that involve memory that is private to said microprocessor, and wherein said partial speculation mode permits handling architectural faults.

Gupta has taught executing according to a partial speculation mode that permits speculation on a first subset of operations and does not permit speculation on a second subset of operations, wherein the partial speculation mode is used in lieu of suspending speculative operations in entirety, and wherein the subset of operations that speculation is permitted upon comprises operations that involve memory that is private to a microprocessor, and wherein said partial speculation mode permits handling architectural

faults *[Gupta; Speculation is permitted on all operations except those that are visible outside of the processor; column 6, line 45 – column 7, line 4]*.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify the method of Dehnert to include executing forward from the speculation boundary according to the partial speculation mode as taught by Gupta. In doing so, the first subset would not include all of the speculative operations. Further, the executing forward would be done according to a partial speculation mode that permits a non-null second subset of said set of speculative operations, wherein said partial speculation mode is used in lieu of suspending said set of speculative operations in entirety, and wherein said second subset comprises operations that involve memory that is private to the microprocessor, and wherein said partial speculation mode permits handling architectural faults.

The motivation for doing so would have been that performance is increased by executing speculatively *[Gupta; column 1, lines 58-59]* while errors generated by operations that affect the state of external hardware are prevented *[Gupta; column 6, line 65 – column 7, line 4]*.

12. Referring to claim 19, Dehnert has taught a computer system comprising:

a main memory *[memory; section 1]*; and

a microprocessor coupled to said main memory *[Crusoe microprocessor; section 1]*;

wherein said computer system implements a first mode of speculative operation *[1st and 2nd paragraph of section 3]* and a second mode in which speculative operations are suspended in entirety *[execution from speculation boundary is done in-order and therefore non-speculatively; section 3.13]*, wherein operation in said first mode permits speculation of a set of speculative operations up to and beyond a commit point at which a state of said microprocessor is committed to memory and wherein operation in said second mode begins after a rollback operation that restores said state, wherein said first mode permits speculative operations comprising operations that involve memory that is private to a microprocessor *[register operations]*, input/output (I/O) writes *[4th paragraph of section 3.4]*, main memory reads *[2nd paragraph of section 3]*, and main memory writes *[2nd paragraph of section 3]*, wherein said first mode permits speculation for non-architectural faults, and wherein the third mode permits speculation for handling architectural faults.

Dehnert has not taught a third mode of partial speculative operation wherein the third mode permits speculative operations comprising operations that involve memory that is private to a microprocessor.

Gupta has taught executing according to a partial speculation mode that permits speculation on a first subset of operations and does not permit speculation on a second subset of operations, wherein the subset of operations that speculation is permitted upon comprises operations that involve memory that is private to a microprocessor *[Gupta; Speculation is permitted on all operations except those that are visible outside of the processor; column 6, line 45 – column 7, line 4]*.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify the method of Dehnert include a third mode of partial speculative operation wherein the third mode permits speculative operations comprising operations that involve memory that is private to a microprocessor.

The motivation for doing so would have been that performance is increased by executing speculatively *[Gupta; column 1, lines 58-59]* while errors generated by operations that affect the state of external hardware are prevented *[Gupta; column 6, line 65 – column 7, line 4]*.

Response to Arguments

13. Applicant's arguments filed 06/20/2008 have been fully considered but they are not persuasive.

14. Applicant argues the novelty/rejection of the claims, in substance that:

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15. These arguments are not found persuasive for the following reasons:

Regarding the Applicant's argument that combining Dehnert and Gupta would render one of the references inoperable for its intended purpose, the examiner disagrees. While, as noted by the Applicant, Dehnert has taught that, following the rollback, the instructions are executed in program order (i.e. non-speculatively), Dehnert does not state that non-speculative execution is required for operation of the invention as a whole. That is, Dehnert does not state that executing instructions speculatively following a rollback would render the invention inoperable. In fact,

Dehnert states that "[f]ollowing a rollback, CMS usually interprets the x86 instructions corresponding to the faulting translation, executing them in the original program order", thereby indicating the possibility of a rollback response other than in order (i.e. non-speculative) instruction execution.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BENJAMIN P. GEIB whose telephone number is (571)272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Benjamin P Geib
Examiner
Art Unit 2181